Amendments to the Claims

1. (Original): A method of forming a trench isolation region comprising:

forming a masking material over a semiconductor substrate; the masking material comprising at least one of tungsten, titanium nitride and amorphous carbon;

forming an opening through the masking material and into the semiconductor substrate effective to form an isolation trench within semiconductive material of the semiconductor substrate;

forming trench isolation material within the isolation trench and over the masking material outside of the trench effective to overfill the isolation trench;

polishing the trench isolation material at least to an outermost surface of the at least one of tungsten, titanium nitride and amorphous carbon of the masking material; and

etching the at least one of tungsten, titanium nitride and amorphous carbon from the substrate.

2. (Original): The method of claim 1 wherein the masking material comprises tungsten.

3. (Original): The method of claim 1 wherein the masking material comprises titanium nitride.

4. (Original): The method of claim 1 wherein the masking material comprises amorphous carbon.

5. (Original): The method of claim 4 wherein the amorphous carbon comprising layer comprises at least one of boron and nitrogen.

6. (Original): The method of claim 4 wherein the amorphous carbon comprising layer is transparent to visible light.

7. (Original): The method of claim 1 wherein the masking material comprises at least two of tungsten, titanium nitride and amorphous carbon.

8. (Original): The method of claim 7 wherein the masking material comprises amorphous carbon.

9. (Original): The method of claim 1 wherein the semiconductive material comprises bulk substrate monocrystalline silicon.

10. (Original): The method of claim 1 wherein the trench isolation material comprises silicon dioxide.

11. (Original): The method of claim 10 wherein the trench isolation material comprise a layer comprising silicon nitride, at least some of the silicon dioxide being formed over the silicon nitride comprising layer.

12. (Original): The method of claim 11 wherein the at least some is formed on silicon nitride of the silicon nitride comprising layer.

13. (Original): The method of claim 1 wherein the etching is conducted selectively to at least some of the trench isolation material.

14. (Original): The method of claim 13 wherein the etching is conducted selectively to all of the trench isolation material.

15. (Original): The method of claim 1 wherein the masking material is void of silicon nitride.

16. (Original): A method of forming a trench isolation region comprising:

forming a masking material over a semiconductor substrate; the masking material comprising at least one of tungsten, titanium nitride and amorphous carbon;

forming an opening through the masking material and into the semiconductor substrate effective to form an isolation trench within semiconductive material of the semiconductor substrate;

forming trench isolation material within the isolation trench and over the masking material outside of the trench effective to overfill the isolation trench, the trench isolation material comprising a silicon nitride comprising layer having at least one material other than silicon nitride formed thereover;

polishing the trench isolation material at least to an outermost surface of the at least one of tungsten, titanium nitride and amorphous carbon of the masking material; and

etching the at least one of tungsten, titanium nitride and amorphous carbon from the substrate substantially selectively to the silicon nitride comprising layer.

17. (Original): The method of claim 16 wherein the masking material comprises tungsten.

18. (Original): The method of claim 16 wherein the masking material comprises titanium nitride.

19. (Original): The method of claim 16 wherein the masking material comprises amorphous carbon.

20. (Original): The method of claim 19 wherein the amorphous carbon comprising layer comprises at least one of boron and nitrogen.

21. (Original): The method of claim 19 wherein the amorphous carbon comprising layer is transparent to visible light.

22. (Original): The method of claim 16 wherein the masking material comprises at least two of tungsten, titanium nitride and amorphous carbon.

23. (Original): The method of claim 22 wherein the masking material comprises amorphous carbon.

24. (Original): The method of claim 16 wherein the etching is conducted selectively to all of the trench isolation material.

25. (Original): The method of claim 16 wherein the masking material is void of silicon nitride.

26. (Original): A method of forming a trench isolation region comprising:

forming masking material over a semiconductor substrate, at least some of the masking material being oxidizable;

forming an opening through the masking material and into the semiconductor substrate effective to form an isolation trench within semiconductive material of the semiconductor substrate, the opening and the isolation trench having respective sidewalls;

exposing the substrate to oxidizing conditions effective to oxidize the masking material sidewalls at a greater rate than which the sidewalls of the semiconductive material are oxidized; and

forming trench isolation material within the isolation trench.

27. (Original): The method of claim 26 wherein forming the trench isolation material comprises forming a silicon nitride comprising layer over the oxidized masking material sidewalls and oxidized semiconductive material sidewalls.

28. (Original): The method of claim 26 wherein the oxidizable masking material comprises polysilicon.

29. (Original): The method of claim 28 wherein the polysilicon is doped with at least one of boron and phosphorus.

30. (Original): The method of claim 28 wherein the semiconductive material of the sidewalls comprises monocrystalline silicon.

31. (Original): The method of claim 28 wherein forming the trench isolation material comprises forming a silicon nitride comprising layer over the oxidized masking material sidewalls and oxidized semiconductive material sidewalls.

32. (Original): The method of claim 28 wherein the masking material comprises at least one of tungsten, titanium nitride and amorphous carbon.

33. (Original): The method of claim 32 wherein the masking material comprises tungsten.

34. (Original): The method of claim 32 wherein the masking material comprises titanium nitride.

35. (Original): The method of claim 32 wherein the masking material comprises amorphous carbon.

36. (Original): The method of claim 35 wherein the amorphous carbon comprising layer comprises at least one of boron and nitrogen.

37. (Original): The method of claim 35 wherein the amorphous carbon comprising layer is transparent to visible light.

38. (Original): The method of claim 28 wherein the masking material comprises at least two of polysilicon, tungsten, titanium nitride and amorphous carbon.

39. (Original): The method of claim 38 wherein the masking material comprises amorphous carbon.

40. (Original): The method of claim 26 wherein the masking material is void of silicon nitride.

41. (Original): The method of claim 26 wherein the trench isolation material comprises high density plasma deposited silicon dioxide.

42. (Original): The method of claim 26 wherein the exposing forms an oxide layer which is laterally thicker over the masking material sidewalls than over the sidewalls of the semiconductive material.

43. (Original): A method of forming a trench isolation region comprising:

forming a masking material over a semiconductor substrate;

forming an opening through the masking material and into the semiconductor substrate effective to form an isolation trench within semiconductive material of the semiconductor substrate;

depositing a silicon nitride comprising layer within the isolation trench and over the masking material effective to line the trench;

depositing trench isolation material over the silicon nitride comprising layer within the isolation trench and over the masking material outside of the trench;

polishing the trench isolation material and the silicon nitride comprising layer at least to the masking material; and

removing the masking material and the trench isolation material relative to the silicon nitride comprising layer from outwardly of semiconductive material of the semiconductor substrate effective to leave a portion of the silicon nitride comprising layer projecting outwardly from semiconductive material of the semiconductor substrate.

44. (Original): The method of claim 43 wherein the masking material is void of silicon nitride.

45. (Original): The method of claim 43 wherein the masking material comprises at least one of polysilicon, tungsten, titanium nitride and amorphous carbon.

46. (Original): The method of claim 45 wherein the masking material comprises polysilicon.

47. (Original): The method of claim 45 wherein the masking material comprises tungsten.

48. (Original): The method of claim 45 wherein the masking material comprises titanium nitride.

49. (Original): The method of claim 45 wherein the masking material comprises amorphous carbon.

50. (Original): The method of claim 49 wherein the amorphous carbon comprising layer comprises at least one of boron and nitrogen.

51. (Original): The method of claim 49 wherein the amorphous carbon comprising layer is transparent to visible light.

52. (Original): The method of claim 45 wherein the masking material comprises at least two of polysilicon, tungsten, titanium nitride and amorphous carbon.

53. (Original): The method of claim 52 wherein the masking material comprises amorphous carbon.